REMARKS

Applicants respectfully solicit favorable reconsideration and thence a notice of allowance.

Claims presented

Applicants submit claims 1-3 and 4-7 and 9 for examination. Amended claim 1 finds support in the specification at page 7, bottom line to page 8, line 9. Claims 4 and 8 have been cancelled.

Traversing the prior art rejections

Applicants respectfully traverse the rejection of claims 1-4 under 35 U.S.. 102(b) over Mori '731 (JP H06-349731A).

Applicants' claims 1-3 (claim 4 has been canceled) are novel because Mori '731 does not disclose or describe the method steps arranged as in these claims. For instance, Mori '731 does not disclose polishing the substrate (1) and a part of the functional layer (2) which is in contact with (1) to remove them. Mori '731 also, as another example, does not disclose bonding a thermally conductive substrate to the exposed surface of the functional layer. **Indeed, Mori '731 does not describe the thermally conductive substrate (4).**

This follows from the English-language abstract to Mori '731. According to the English-language abstract, a GaAs buffer layer 2 and a first InP contact layer 3 are successively formed on an Si substrate 1 (see "(a)" in Abstract). An InGaAs spacer layer 5, InP device layer 6, second contact layer 7 are successively formed on an InP substrate 4 (see "(a)" in Abstract). Then the laminated structures on substrates 1 and 4 are put together by putting the first and second InP contact layers 3 and 7 upon each other (see "(b)" in Abstract) and they are made to adhere to each other by applying pressure while they are subjected to heat treatment. Finally, the device layer 6 is exposed by removing the substrate 4 and other layers, such as spacer layer 5.

Nonetheless, and subject to correction if the Examiner makes an English translation available, for the sake of argument (*arguendo*), it appears from the Mori '731 Japanese figures that the reference does not disclose Applicants' claimed processes. *Arguendo*, from Fig. 4(a) in the Japanese text for Mori '731, it appears that a first GaAS buffer layer 31, a first InP contact layer 3, and InP device layer 6, a second InGaAs spacer 32, a first InP layer 21 are grown on an InP substrate

4. It may be by MBE. A GaAs buffer layer 2 and a second InP layer 25 apparently are grown on an Si support substrate 41. A GaAs device layer 24 and a second InP contact layer 7 are apparently grown on substrate 1. It then appears that P is removed from the first InP layer 21 and the second InP layer 25 – by heating, it would appear – to be a first metal In layer 26 and a second In metal layer as apparently illustrated in Fig. 4(b) in the Mori '731 Japanese text. The first In layer 26 is bonded to the second In layer 27 at a temperature apparently not less than the melting temperature of In. *Arguendo,* InP substrate 4 and the first InGaAs spacer layer 31 are selectively polished and etched to remove them, and the lower surface of the first InP contact layer 3 is exposed, apparently as shown in Fig. 4(c) in the Mori '731 Japanese text. *Arguendo,* after surface treatment with HF and sulfuric acid, binding the second InP contact layer 7 with the first InP contact layer 3 is performed, and apparently subjected to heat treatment, presumably under a hydrogen atmosphere, which might as illustrated in the Mori '731 Japanese Fig. 4(d). *Arguendo*, the surface of the InP device is exposed, as in Mori '731 Fig. 4(e) in the Japanese text, by polishing and selectively etching the Si support substrate 41, the GaAs buffer layer 2, the second metal In layer 27, the first In metal layer 26, and the second InGaAs spacer layer 32.

Applicants respectfully traverse the rejection of claims 5-9 under 35 U.S.C. 102(e) over Sano (U.S. Patent No. 6,916,676).

Sano '676 does not disclose or describe the method according to Applicants' claims 5-9. For instance, Sano '676 does not describe the claim 5 method including step (h), in which polishing a part of the compound semiconductor functional layer (22) on the side that is in contact with the substrate (21) to remove them is provided. Furthermore, Sano '676 does not disclose the thermally conductive substrate (4).

Therefore, claims 5-7 and 9 each defines a novel invention over Sano.

Applicants respectfully submit their claim 9 defines an unobvious invention over Mori '731. Applicants point out that Mori '731 does not describe, nor would it have suggested claim 1, and therefore would not have suggested the subject invention defined by linking claim 9.

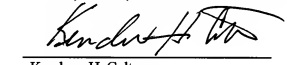
Conclusion:

Applicants have responded to all matters presented in the Office Action and respectfully submit their claims 1-3 define novel inventions over Mori '731, claims 5-9 define novel inventions over Sano '676, and claim 9 defines an unobvious invention over Mori '731. A Notice of Allowance is courteously solicited.

Applicants hereby request a three-month extension of time. The Commissioner is hereby authorized to charge the $1,110 three-month extension fee to Deposit Account No. 06-1135. The Commissioner is further authorized to charge any required fee not intentionally omitted, including application processing, extension, extra claims, statutory disclaimer, issue, and publication fees, to said Deposit Account No. 06-1135 in connection with Order No. 7372/88130.

Respectfully submitted,

FITCH, EVEN, TABIN & FLANNERY



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